REMARKS

The Office Action dated May 15, 2008 has been reviewed and carefully considered. Claims 1-6 have been amended. Claim 8, combining the features of claims 1 and 4, has been added. The features of newly added dependent claims 9-10 and 11-13 correspond to the features of claims 2-3 and 5-7, respectively. Claims 1 and 8 are the only independent claims. Reconsideration of the above-identified application, as amended and in view of the following remarks, is respectfully requested.

Applicant notes with appreciation the indication that claims 4 and 5 would be allowable if rewritten so as not to depend from a rejected claim, and with no change in scope. Claim 4 has been so rewritten as newly added claim 8, and accordingly is now believed to be in condition for allowance. Claims 9-13, which depend from claim 8, are also believed allowable based on their dependence from claim 8.

Claims 1-3 and 6-7 stand rejected under 35 USC 102(b) as being anticipated by Gupta, U.S. Patent No. 5,353,248 (Hereinafter "Gupta").

Gupta's invention "relates to static random access memories (SRAMs), and more particularly, to backing up SRAMs with electrically erasable programmable read-only memories (EEPROMs) when SRAMs are used as first-in first-out (FIFO) serial memory devices" (col. 1, lines 5-10). As described by Gupta throughout his patent, SRAM's are volatile devices for which backup storage is required: "SRAMs, by their nature, are

volatile devices (i.e., they lose the stored information when the circuit is unpowered). Therefore, the controlling data must be re-written into them on each power-up operation" (col. 1, lines 17-18). Gupta deals with this problem in the prior art by combining EEPROM elements to provide a non-volatile backup to SRAM elements.

The present invention relates to addressing prior art problems associated with static FIFO devices. By way of example, paragraphs [0006] to [0008] describe the problems associated with latency in such devices. This problem is addressed by the present invention by:

> [adding] additional stages [which] are **volatile (or dynamic)** FIFOs [emphasis added]. In accordance with a first aspect of the present invention, there is provided a FIFO memory device comprising a storage stage and input stage, the storage stage comprising a plurality of non-volatile storage elements and the input stage comprising a plurality of volatile storage elements. In this way the input stage effectively hides the latency of the storage stage.

As is well known in the art, dynamic RAM (DRAM), needs to be periodically refreshed. Static RAM (SRAM) exhibits data remanence. However, SRAM can be regarded as "volatile" in the sense that data would be lost when power is lost to the memory device. While the specification (e.g., paragraph [0012]) clearly defines SRAM as being non-volatile memory and DRAM as being volatile memory; in the interests of furthering prosecution, Applicant has amended claim 1 to include the terms "static" and "dynamic" to more clearly define what is intended by the terms "non-volatile" and "volatile," respectively. In particular, claim 1 as amended recites:

A FIFO memory device comprising a storage stage and input stage, the storage stage comprising a plurality of static, non-volatile storage elements and the input stage comprising a plurality of dynamic, volatile storage elements.

Gupta fails to teach the invention as claimed. In particular, and as noted by the Examiner, the input stage of Gupta is an SRAM cell (1st sentence of paragraph 4 of the Office Action, referencing Fig. 2 of Gupta). Accordingly, Gupta teaches away from the present invention wherein the input state comprises dynamic storage elements (e.g., DRAM).

A claim is anticipated only if each and every element recited therein is expressly or inherently described in a single prior art reference. Gupta cannot be said to anticipate the present invention, because Gupta fails to disclose each and every element recited. As shown, Gupta fails to disclose the limitations of "the input stage comprising a plurality of dynamic, volatile storage elements" as is recited in claim 1.

Having shown that Gupta fails to disclose each and every element claimed, applicant submits that claim 1 is allowable over Gupta. Applicant respectfully requests reconsideration, withdrawal of the rejection and allowance of claim 1.

With regard to claims 2-7, these claims ultimately depend from claim 1, which has been shown to be not anticipated and allowable in view of the cited references. Accordingly, claims 2-7 are also allowable by virtue of their dependence from an allowable base claim.

For all the foregoing reasons, it is respectfully submitted that all the present claims are patentable in view of the cited references. A Notice of Allowance is respectfully requested.

Respectfully submitted,

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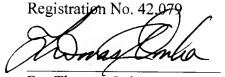

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